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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/643,397	08/19/2003	Paul John Mantey	200312864-1	3980	
22879	7590 08/23/2005		EXAMI	EXAMINER	
	PACKARD COMPANY	DIMYAN, I	DIMYAN, MAGID Y		
P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION			ART UNIT	PAPER NUMBER	
FORT COLLI	NS, CO 80527-2400		2825		
			DATE MAILED: 08/23/2005	;	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)				
Office Action Summary		10/643,397	MANTEY ET AL.	(AM)			
		Examiner	Art Unit				
		Magid Y. Dimyan	2825				
	ATE of this communication app	ears on the cover sheet with the c	orrespondence addre	ess			
THE MAILING DATE (- Extensions of time may be av after SIX (6) MONTHS from the - If the period for reply specified - If NO period for reply is specified - Failure to reply within the set - Any reply received by the Offi earned patent term adjustmen	OF THIS COMMUNICATION. ailable under the provisions of 37 CFR 1.13 ne mailing date of this communication. d above is less than thirty (30) days, a reply field above, the maximum statutory period w or extended period for reply will, by statute, ce later than three months after the mailing	'IS SET TO EXPIRE 3 MONTH() 6(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days ill apply and will expire SIX (6) MONTHS from the cause the application to become ABANDONED date of this communication, even if timely filed	ety filed s will be considered timety. the mailing date of this comm O (35 U.S.C. § 133).	nunication.			
Status							
1)⊠ Responsive to α	ommunication(s) filed on <u>19 Au</u>						
2a) This action is FI	• • •	action is non-final.					
•	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
4a) Of the above 5) ☐ Claim(s) is 6) ☑ Claim(s) <u>1-20</u> is 7) ☐ Claim(s) is							
Application Papers							
•	is objected to by the Examiner	r. a)⊠ accepted or b)⊡ objected t	a hu tha Evaninas				
		a)l⊠ accepted of b)∟ objected t drawing(s) be held in abeyance. See	•				
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_		aminer. Note the attached Office					
Priority under 35 U.S.C. §	119						
a) All b) Som 1. Certified of 2. Certified of 3. Copies of tapplication	e * c) None of: opies of the priority documents opies of the priority documents the certified copies of the priori of from the International Bureau	have been received in Application to the have been received ity documents have been received	on No d in this National Sta	age			
Attachment(s) 1) Notice of References Cited 2) Notice of Draftsperson's Pa 3) Information Disclosure Stat Paper No(s)/Mail Date 8/19	atent Drawing Review (PTO-948) ement(s) (PTO-1449 or PTO/SB/08)	4) Interview Summary (Paper No(s)/Mail Da 5) Notice of Informal Pa 6) Other:	te	(2)			

Application/Control Number: 10/643,397

Art Unit: 2825

DETAILED ACTION

1. This is with regards to Application No. 10/643,397 filed 19 August 2003. Claims 1

– 20 remain pending in this Application.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Art Unit: 2825

2. Claims 1, 13 and 19 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,898,775. Although the conflicting claims are not identical, they are not patentably distinct from each other because the "circuit designs" of the pending application is obviously the "printed circuit boards" of the '775 patent, while the "connections of circuit designs" is obviously the "pin assignments" of '775.

- 3. Claims 5, 6 and 7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 3 and 4, respectively of U.S. Patent No. 6,898,775. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 5 teaches the elements of user interface coupled to user stations (similar to claim 2 of the '775 patent); claim 6 teaches the elements of configuration files comprising symbol files (similar to claim 4 of the '775 patent); and claim 7 teaches the element of configuration files comprising geometry files (similar to claim 5 of the '775 patent).
- 4. Claim 14 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 4 and 5, collectively, of U.S. Patent No. 6,898,775. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 14 teaches the similar elements of configuration

Art Unit: 2825

files having one or both of symbol files and geometry files (same as in claim 4 and 5 of the '775 patent).

5. Claims 2 - 4, 8 - 12, 15 - 18 and 20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 5 of U.S. Patent No. 6,898,775 in view of U.S. Publication No. 2003/0084418 to Regan. These claims pertain to mapping file generated from a list of interconnectivity signals, user interface, updating the mapping file, and generating a schematic which are made obvious by Regan (see (9) – (18) below).

Specification

6. The disclosure is objected to because of the following informalities: Paragraph 0001 should be corrected to include the issued U.S. Patent No. 6,629,307.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

Art Unit: 2825

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

- 8. Claims 1 3 and 6 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Publication No. 2003/0084418 to Regan.
- 9. Pursuant to claims 1, 13, 17 and 19, Regan discloses a process for modifying the design of IC circuits that includes ensuring connectivity between circuit designs (see page 1, paragraphs 0017, 0071), and comprising: (a) configuration files defining connections of the circuit designs and at least one mapping file correlating connections between the configuration files (see Figs. 5, 14a, 17, 24; paragraphs 0077- 0097, which collectively teach how to map and configure a design); and (b) a processing section for updating the mapping file in response to changes of the circuit designs and for processing the configuration files and the mapping file in generating the circuit design (see paragraphs 0144 0153 which cite how the mapping and configuration of the circuit can be modified). Thus, Regan discloses all the claimed limitations.
- 10. As per claims 2 and 3, see (9) above; Fig. 3, Fig. 24 (block 134), and paragraphs 0077 0090, which collectively show how a list of interconnectivity signals is used to generate the mapping file, as claimed.

Art Unit: 2825

11. Referring to claims 6 and 7, see Figs. 17, 21a, 21b, 21c, 22a, 23a, which show the claimed elements of using symbol files and geometry files to represent parts within the circuit designs.

- 12. Regarding claims 8 12, see (9) above, as well as Fig. 24; paragraphs 0003 0007, 0144 0147 and 0153 which recite the claimed limitations pertaining to updating the mapping files when a design change or connectivity change is warranted.
- 13. Claim 14 contains the same limitations found in claims 4 and 5, and thus the same rejections also apply.
- 14. Claims 15 and 16 have the same limitations as in claims 2 and 3, respectively, and the same rejections apply.
- 15. Claims 18 and 20 contain the same limitations as in claim 9, and thus the same rejections also apply.

Claim Rejections - 35 USC § 103

- 16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Art Unit: 2825

17. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Regan in view of Zizzo (U.S. Patent No. 6,578,174).

18. The teachings of Regan pertaining to a process for modifying and verifying connectivity between circuit designs are cited above, and described in detail in his disclosure. However, Regan is silent on the use of a user interface for connection to one or more user stations in generating interconnectivity signals or inputting the changes to the circuit designs as claimed. On the other hand, Zizzo discloses a multi-faceted circuit design platform to facilitate circuit design that makes use of a network with a plurality of user stations (see Figs. 1, 2 and 6) as well as a user interface (see Figs. 8A -C). Employing a user interface and one or more user stations are now very commonly used in IC circuit development because of today's complex designs. It would therefore be obvious to a person of ordinary skill in the art to combine the teachings of Regan and Zizzo to obtain the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan Examiner Art Unit 2825

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10 August 2005

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